REMARKS

Claims 1 - 14 remain active in this application. Claims 1 - 5 have been withdrawn from consideration as being non-elected, with traverse, in response to a requirement for election of species. The specification has been reviewed and editorial revisions made where seen to be appropriate. Claims 6, 10, 11 and 14 have been amended. Support for the amendments of the claims is found throughout the application, particularly in Figures 4 - 7 and the description thereof in paragraphs 37 - 44 and paragraphs 37 - 39 and 41 in particular. No new matter has been introduced into the application.

The Examiner has adhered to the requirement for election of species. However, the traverse of the requirement is respectfully maintained. It was previously pointed out in the response filed June 9, 2006, that the requirement was incomplete. The Examiner's further comments in the present office action merely indicated that there are some recitations in the claims corresponding to Species I as identified by the Examiner which are not in the claims corresponding to Species II. However, it respectfully submitted that it does not necessarily follow that those differences in recitations between the claims would require different fields of search, particularly when it is understood that Species I is directed to optimization of chip size of an integrated circuit design which the apparatus claims of Species II are directed to a chip structure which would result from such optimization. For that reason alone, it appears that the searches for the respective species as identified by the Examiner would tend to be congruent rather than divergent and, indeed, the Examiner has not asserted different classification for the respective

species and therefore it is assumed that the Examiner has determined that they would, in fact, be commonly classified. Further, the Examiner has not answered other points of incompleteness of the requirement previously pointed out in the response filed June 9, 2006. Therefore, it is again respectfully submitted that the requirement is improper and, upon reconsideration, should be withdrawn.

The Examiner has objected to recitations contained in claims 6 and 14 without citing any authority or reason therefor other than Applicant's intentions in regard to that language are unclear. This objection is respectfully traversed since there is no requirement that the claims *explain* the invention but only to define it in a manner distinct from the prior art and such that the scope of the claims can be reasonably determined. It is respectfully submitted that there is no ambiguity engendered by the language which the Examiner criticizes. Nevertheless, both claims 6 and 14 have been amended to ensure that the definition of the invention provided in the claims is abundantly clear to the Examiner, particularly since the Examiner's asserted confusion in regard to the criticized recitations appears to underlie several asserted grounds of rejection with which the Examiner appears to have sought to improperly buttress other improper grounds of rejection. Therefore, since the claims, as amended, are abundantly clear in regard to the criticized recitations, reconsideration and withdrawal of this objection is respectfully requested.

Claim 6 has been rejected under 35 U.S.C. §112, first paragraph, as being inadequately supported by enabling disclosure in regard to the recitation that an I/O kernel is "independent of any other I/O Kernel" (the same language criticized in the objection discussed

above). This ground of rejection is respectfully traversed.

It is respectfully submitted that when the punctuation of claim 6 is properly observed, the questioned language of original claim 6 clearly and unambiguously refers to common power connections of the I/O cells which comprise a given I/O kernel and determine the articulation between I/O kernels. That is, the I/O cells for which the power connection are common comprise and define a given I/O kernel which is, conversely, differentiated from another I/O kernel having different power connections for the given I/O kernel but which are, nevertheless, common among the I/O cells included therein. This subject matter is clearly supported by numerous passages of the original disclosure and is set out with particular clarity in the last sentence of paragraph 39. Therefore, it is respectfully submitted that this ground of rejection is clearly in error as to the original claim language and particularly untenable in view of the amendments made thereto. Therefore, reconsideration and withdrawal of this ground of rejection are respectfully requested.

Claims 6 - 11, 13 and 14 have been rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter and lacking patentable utility. This ground of rejection is also respectfully traversed.

It is respectfully submitted that all the claims included within this ground of rejection are directed to an integrated circuit structure having particular structural and layout features which are manifestly statutory subject matter and which clearly have utility since the claimed features allow use of standard integrated circuit patterns for I/O cell and I/O kernel layout which can be altered to minimize the size of chip

required for a given number of I/O cells, logic cells and other types of cells needed for a given functionality required from a given integrated circuit. Such a result is inherently and unquestionably useful (e.g. in avoiding duplicative design effort as well as providing a functional, and thus useful, integrated circuit which additionally allows efficient use of wafer space and reduction of manufacturing costs) while the integrated circuit itself is necessarily concrete and tangible. Therefore, it is respectfully submitted that this ground of rejection is completely without basis in fact or substance and, upon reconsideration should be withdrawn. Further, it appears that the Examiner may be asserting that the claims are drawn to abstract functions or definitions based upon the asserted lack of understanding of recitations of the invention as discussed above and/or to improperly buttress other asserted grounds of rejection. Since claims 6 and 14 have been amended to increase clarity as discussed above, it is respectfully submitted that this ground of rejection is particularly untenable in the regard to the claims as now amended.

Claims 6 - 14 have been rejected under 35 U.S.C. §102 as being anticipated by Ali et al. This ground of rejection is also respectfully traversed, particularly as being moot in view of the amendments made above.

As alluded to above, claims 6 - 14 are directed to an integrated circuit in which I/O cell patterns are depopulated from a standard pattern including power and I/O signal connection patterns to which off-chip connections can be made and in which unneeded I/O cells are depopulated in accordance with I/O kernels in which I/O cells are contiguous and have a common power supply while leaving structures for off-chip connections which would otherwise be used for connections to I/O cells.

Thus the chip area corresponding to unneeded and depopulated contiguous I/O cells can be more readily and efficiently be populated with other types of cells (which are generally of a different size and possible aspect ratio from the I/O cells) such as logic cells while allowing the chip size to be optimized and while retaining all or a portion of the pattern of off-chip connection structures that correspond to depopulated I/O cell sites for powering the cells placed in the depopulated I/O cell sites and other cells included in the core area of the chip.

It is respectfully submitted that Ali et al. teaches little beyond the "Related Art" approaches to chip layout discussed in relation to Figures 1 - 3 of the present application. In fact, Figures 1 and 2 of Ali et al. largely correspond to Related art Figures 2 and 3 of the present application in respectively showing I/O cells alternated with substantially unusable space and I/O cells of altered aspect ratio, respectively; both with so-called in-line (e.g. single row) off-chip connection pads. Similarly, Figure 3 and 4 of Ali et al. largely corresponds to Figure 1 of the present application having an increased number of I/O cells interleaved with the I/O cells of Figure 1 of Ali et al. and having a so-called staggered array of connection pads. Figure 7 of Ali et al. also teaches a technique for increasing the number of I/O cells by providing concentric arrays thereof. That is, Figures 1 - 4 and 7 illustrate techniques for *increasing the number of usable I/O cells* rather than depopulating them from a standard pattern.

In Figures 5 and 6 of Ali et al. the number of I/O cells is reduced compared with, for example, the patterns of Figures 3 and 2 of Ali et al. However, there is no teaching or suggestion of depopulating I/O sites in

accordance with kernels which have common power connections to the I/O cells therein which are independent of the power connections to other I/O kernels and, moreover, Ali et al. also teaches removal of the off-chip connection structures that correspond to the removed I/O cells. In this latter regard, Ali et al. refers to areas 58 as being used for "core logic" which, as a term of art, infers that no off-chip connections are made thereto (since off-chip signal connections are made through I/O cells which remain and there is no teaching seen in Ali et al. of how power is to be supplied to the core logic). Further, Ali et al. certainly does not contemplate using off-chip connection structures associated with I/O cells which have been depopulated in order to supply power to core logic (58). Moreover, the number of required power connections is increasing in many modern integrated circuit designs which operate at reduced voltage and increased current; a problem which Ali et al. does not address.

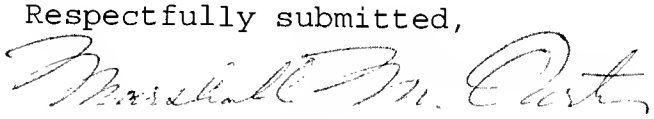
Therefore, it is respectfully submitted that at least original claim 14 , as currently rejected, is not anticipated by Ali et al. and no claim in the application, as amended above, is anticipated by Ali et al. Accordingly, it is respectfully requested that this ground of rejection (as well as the grounds of rejection with which the Examiner appears to improperly seek to buttress it) be reconsidered and withdrawn.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon

reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0456 of International Business Machines Corporation (Burlington).

Respectfully submitted,



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